## ABSTRACT

A high-density flash EEPROM (Electrically Erasable Programmable Read Only Memory) unit cell and a memory array architecture including the same are disclosed. The flash EEPROM unit cell comprises a substrate on which field oxide layers are formed for isolating unit cells, a floating gate dielectric layer formed between the adjacent field oxide layers, wherein the floating gate dielectric layer includes a first dielectric layer and a second dielectric layer which are connected in parallel between a source and a drain formed on the substrate, and the thickness of the first dielectric layer is thicker than the second dielectric layer, a floating gate formed on the floating gate dielectric layer, a control gate dielectric layer formed on the floating gate; and a control gate formed on the control gate dielectric layer.